IN THE CLAIMS:

New claims 21 through 29 have been added. None of the claims have been amended herein. All of the pending claims 1 through 29 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously Presented) An assembly having multiple substrates and a plurality of semiconductor dice located on the multiple substrates, comprising:

a base substrate having a first surface including a plurality of bond pads and a plurality of circuits connected to the plurality of bond pads;

at least one first semiconductor die having an active surface having at least one bond pad thereon and having a second surface;

a first stacked substrate having a first surface, having a second surface, and having a plurality of circuits, the at least one first semiconductor die electrically connected to the first surface of the first stacked substrate and having the second surface thereof disposed on at least one portion of the first surface of the first stacked substrate;

at least one second semiconductor die having a first surface having a plurality of bond pads located thereon, the second surface of the at least one second semiconductor die attached to at least one portion of the second surface of the first stacked substrate;

at least one first connector connecting the at least one bond pad of the at least one first semiconductor die to at least one bond pad of the plurality of bond pads of the base substrate;

at least one second connector connecting at least one bond pad of the plurality of bond pads of the at least one second semiconductor die to at least one other bond pad of the plurality of bond pads of the base substrate;

a second stacked substrate having a first surface, having a second surface, and having a plurality of circuits;

at least one third semiconductor die having a first surface having a plurality of bond pads located thereon, the second surface of the at least one third semiconductor die attached to at least one portion of the first surface of the second stacked substrate; and

at least one third connector connecting at least one bond pad of the plurality of bond pads of the at least one third semiconductor die to the second surface of the first stacked substrate.

2. (Previously Presented) The assembly of claim 1, wherein the at least one first semiconductor die is located on the at least one portion of the first surface of the first stacked substrate being electrically connected to the first stacked substrate thereat.

3. (Previously Presented) The assembly of claim 1, wherein the second surface of the first stacked substrate includes a plurality of bond pads and wherein the at least one second semiconductor die is located on and electrically connected to the at least one portion of the second surface of the first stacked substrate.

4. (Previously Presented) The assembly of claim 1, wherein the at least one first connector includes one of solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

5. (Previously Presented) The assembly of claim 1, wherein the base substrate further comprises a second surface having a plurality of bond pads located thereon.

6. (Previously Presented) The assembly of claim 5, further comprising connections attached to the plurality of bond pads of the second surface of the base substrate for connection with external electrical circuitry.

7. (Previously Presented) The assembly of claim 6, further comprising a plurality of trace leads located on the base substrate connecting the plurality of bond pads of the first surface of the base substrate and the plurality of bond pads of the second surface of the base substrate.

8. (Previously Presented) The assembly of claim 1, further comprising:

a base semiconductor die having a plurality of bond pads and disposed on the base substrate first surface; and

at least one fourth connector connecting the at least one of the plurality of bond pads of the first surface of the base substrate and the at least one bond pad of the base semiconductor die.

9. (Previously Presented) An assembly having a plurality of substrates and having a plurality of semiconductor dice comprising:

a base substrate having a first surface including a plurality of bonds pads thereon, a second surface including a plurality of bond pads thereon, and a plurality of traces, at least one trace of the plurality of traces connecting at least one bond pad of the plurality of bond pads on the first surface of the base substrate to at least one bond pad of the plurality of bond pads on the second surface of the base substrate;

a first stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces connecting at least one bond pad of the plurality of bond pads on the first surface of the first stacked substrate to at least one bond pad of the plurality of bond pads on the second surface of the first stacked substrate, and a second plurality of traces, at least one trace of the second plurality of traces connected to another bond pad of the plurality of bond pads on the first surface of the first stacked substrate;

a first semiconductor die disposed on the first surface of the first stacked substrate, the first semiconductor die connected to the at least one trace of the second plurality of traces connected to the another bond pad of the plurality of bond pads on the first surface of the first stacked substrate;

a second stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces of the second stacked substrate connecting at least one bond pad of the plurality of bond pads on the first surface of the second stacked substrate to at least one bond pad of the plurality of bond pads on the second surface of the second stacked substrate, and a second plurality of traces, at least one trace of the

second plurality of traces of the second stacked substrate connected to another bond pad of the plurality of bond pads on the first surface of the second stacked substrate;

a second semiconductor die disposed on the first surface of the second stacked substrate, the second semiconductor die connected to the at least one trace of the second plurality of traces of the second stacked substrate connected to the another bond pad of the plurality of bond pads on the first surface of the second stacked substrate;

a third semiconductor die disposed on the second surface of the second stacked substrate;

a first plurality of connections connecting the base substrate and the first stacked substrate, at least one connection of the first plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the base substrate to the at least one bond pad of the plurality of bond pads on the first surface of the first stacked substrate, the first plurality of connections connecting the base substrate and the first stacked substrate supporting the first stacked substrate;

a second plurality of connections connecting the second stacked substrate and the first stacked substrate, at least one connection of the second plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the second stacked substrate to the at least one bond pad of the plurality of bond pads on the second surface of the first stacked substrate, the second plurality of connections connecting the first stacked substrate and the second stacked substrate supporting the second stacked substrate;

a third stacked nonconductive substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces of the third stacked nonconductive substrate connecting at least one bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate to at least one bond pad of the plurality of bond pads on the second surface of the third stacked nonconductive substrate, and a second plurality of traces, at least one trace of the second plurality of traces of the third stacked nonconductive substrate connected to another bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate;

a fourth semiconductor die disposed on the second surface of the third stacked nonconductive substrate;

a fifth semiconductor die disposed on the first surface of the third stacked nonconductive substrate, the fifth semiconductor die connected to the at least one trace of the second plurality of traces of the third stacked nonconductive substrate connected to the another bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate; and

a third plurality of connections connecting the third stacked nonconductive substrate and the second stacked substrate, at least one connection of the third plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate to the at least one bond pad of the plurality of bond pads on the second surface of the second stacked substrate.

10. (Previously Presented) The assembly of claim 9, wherein the first plurality of connections includes solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

11. (Previously Presented) The assembly of claim 9, wherein the second plurality of connections includes solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

12. (Previously Presented) The assembly of claim 9, further comprising:

a fourth plurality of connections, at least one connection of the fourth plurality of connections connecting the at least one bond pad of the plurality of bond pads on the second surface of the base substrate to external electrical circuitry.

13. (Previously Presented) The assembly of claim 9, wherein the first semiconductor die disposed on the first surface of the first stacked substrate is connected to the at least one trace of the second plurality of traces connected to the another bond pad of the plurality of bond pads

on the first surface of the first stacked substrate through one of flip chip attachment, wirebonding, TAB tape, and a combination thereof.

14. (Previously Presented) The assembly of claim 9, wherein the second semiconductor die disposed on the first surface of the second stacked substrate is connected to the at least one trace of the second plurality of traces of the second stacked substrate connected to the another bond pad of the plurality of bond pads on the first surface of the second stacked substrate through one of flip chip attachment, wirebonding, TAB tape, and a combination thereof.

15. (Previously Presented) The assembly of claim 9, wherein the third semiconductor die disposed on the second surface of the second stacked substrate is connected to the at least one bond pad of the plurality of bond pads on the second surface of the second stacked substrate.

16. (Previously Presented) The assembly of claim 9, wherein the third semiconductor die disposed on the second surface of the second stacked substrate is connected to the at least one bond pad of the plurality of bond pads on the first surface of the second stacked substrate.

17. (Previously Presented) The assembly of claim 9, wherein the second semiconductor die disposed on the first surface of the second stacked substrate is connected to the at least one bond pad of the plurality of bond pads on the second surface of the second stacked substrate and wherein the third semiconductor die disposed on the second surface of the second stacked substrate is connected to the at least one bond pad of the plurality of bond pads on the second surface of the second stacked substrate.

18. (Previously Presented) The assembly of claim 9, further comprising:

a fourth stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces of the fourth stacked substrate connecting at least one bond pad of the plurality of bond pads on the first surface of the fourth stacked

substrate to at least one bond pad of the plurality of bond pads on the second surface of the fourth stacked substrate, and a second plurality of traces, at least one trace of the second plurality of traces of the fourth stacked substrate connected to another bond pad of the plurality of bond pads on the first surface of the fourth stacked substrate, the fourth stacked substrate located above the second stacked substrate, the fourth stacked substrate having a size less than sizes of the base substrate, the first stacked substrate, the second stacked substrate, and the third stacked nonconductive substrate;

a sixth semiconductor die disposed on the first surface of the fourth stacked substrate, the sixth semiconductor die connected to the at least one trace of the second plurality of traces of the fourth stacked substrate connected to the another bond pad of the plurality of bond pads on the first surface of the fourth stacked substrate; and

a fourth plurality of connections connecting the fourth stacked substrate and the second stacked substrate, at least one connection of the fourth plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the fourth stacked substrate to the at least one bond pad of the plurality of bond pads on the second surface of the second stacked substrate.

19. (Previously Presented) An assembly having a plurality of substrates and having a plurality of semiconductor dice comprising:

a base substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, and a plurality of traces, at least one trace of the plurality of traces connecting at least one bond pad of the plurality of bond pads on the first surface of the base substrate to at least one bond pad of the plurality of bond pads on the second surface of the base substrate;

a first stacked substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces connecting at least one bond pad of the plurality of bond pads on the first surface of the first stacked substrate to at least one bond pad of the plurality of bond pads on the second surface of the first stacked substrate, and a second

plurality of traces, at least one trace of the second plurality of traces connected to another bond pad of the plurality of bond pads on the first surface of the first stacked substrate;

a plurality of first semiconductor dice disposed on the first surface of the first stacked substrate, each die of the plurality of first semiconductor dice connected to the at least one trace of the second plurality of traces connected to the another bond pad of the plurality of bond pads on the first surface of the first stacked substrate;

a second stacked nonconductive substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces of the second stacked nonconductive substrate connecting at least one bond pad of the plurality of bond pads on the first surface of the second stacked nonconductive substrate to at least one bond pad of the plurality of bond pads on the second surface of the second stacked nonconductive substrate, and a second plurality of traces, at least one trace of the second plurality of traces of the second stacked nonconductive substrate connected to another bond pad of the plurality of bond pads on the first surface of the second stacked nonconductive substrate;

a plurality of second semiconductor dice disposed on the first surface of the second stacked nonconductive substrate, each die of the plurality of second semiconductor dice connected to the at least one trace of the second plurality of traces of the second stacked nonconductive substrate connected to the another bond pad of the plurality of bond pads on the first surface of the second stacked nonconductive substrate;

a plurality of third semiconductor dice disposed on the second surface of the second stacked nonconductive substrate;

a first plurality of connections connecting the base substrate and the first stacked substrate, at least one connection of the first plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the base substrate to the at least one bond pad of the plurality of bond pads on the first surface of the first stacked substrate, the first plurality of connections connecting the base substrate and the first stacked substrate supporting the first stacked substrate;

a second plurality of connections connecting the second stacked nonconductive substrate and the first stacked substrate, at least one connection of the second plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the second stacked nonconductive substrate to the at least one bond pad of the plurality of bond pads on the second surface of the first stacked substrate;

a third stacked nonconductive substrate having a first surface including a plurality of bond pads thereon, a second surface including a plurality of bond pads thereon, a first plurality of traces, at least one trace of the first plurality of traces of the third stacked nonconductive substrate connecting at least one bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate to at least one bond pad of the plurality of bond pads on the second surface of the third stacked nonconductive substrate, and a second plurality of traces, at least one trace of the second plurality of traces of the third stacked nonconductive substrate connected to another bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate;

a plurality of fourth semiconductor dice disposed on the first surface of the third stacked nonconductive substrate, each die of the plurality of fourth semiconductor dice connected to the at least one trace of the second plurality of traces of the third stacked nonconductive substrate connected to the another bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate;

a plurality of fifth semiconductor dice disposed on the second surface of the third stacked nonconductive substrate; and

a third plurality of connections connecting the third stacked nonconductive substrate and the second stacked nonconductive substrate, at least one connection of the third plurality of connections connecting the at least one bond pad of the plurality of bond pads on the first surface of the third stacked nonconductive substrate to the at least one bond pad of the plurality of bond pads on the second surface of the second stacked nonconductive substrate.

20. (Previously Presented) The assembly of claim 19, wherein the first plurality of connections and second plurality of connections includes one of solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

Please add the following new claims:

21. (New) An assembly of substrates and semiconductor dice comprising:

a base substrate having a first surface including a plurality of bond pads and a plurality of circuits connected to the plurality of bond pads;

a first semiconductor die having an active surface having at least one bond pad thereon and having a second surface;

a first stacked substrate having a first surface, having a second surface, and having a plurality of circuits, the first semiconductor die electrically connected to the first surface of the first stacked substrate and having the second surface thereof disposed on at least one portion of the first surface of the first stacked substrate;

a second semiconductor die having a first surface having a plurality of bond pads located thereon, the second surface of the at least one second semiconductor die attached to at least one portion of the second surface of the first stacked substrate;

a first connector connecting the at least one bond pad of the at least one first semiconductor die to at least one bond pad of the plurality of bond pads of the base substrate; and

a second connector connecting at least one bond pad of the plurality of bond pads of the at least one second semiconductor die to at least one other bond pad of the plurality of bond pads of the base substrate.

22. (New) The assembly of claim 21, further comprising:

a second stacked substrate having a first surface, having a second surface, and having a plurality of circuits;

a third semiconductor die having a first surface having a plurality of bond pads located thereon, the second surface of the third semiconductor die attached to at least one portion of the first surface of the second stacked substrate; and

a third connector connecting at least one bond pad of the plurality of bond pads of the at least one third semiconductor die to the second surface of the first stacked substrate.

23. (New) The assembly of claim 21, wherein the first semiconductor die is located on the at least one portion of the first surface of the first stacked substrate being electrically connected to the first stacked substrate thereat.

24. (New) The assembly of claim 21, wherein the second surface of the first stacked substrate includes a plurality of bond pads and wherein the second semiconductor die is located on and electrically connected to the at least one portion of the second surface of the first stacked substrate.

25. (New) The assembly of claim 21, wherein the first connector includes one of solder, conductive adhesives, Z-axis conductive material, flex-contacts, spring contacts, wire bonds, and TAB tape.

26. (New) The assembly of claim 21, wherein the base substrate further comprises a second surface having a plurality of bond pads located thereon.

27. (New) The assembly of claim 26, further comprising connections attached to the plurality of bond pads of the second surface of the base substrate for connection with external electrical circuitry.

28. (New) The assembly of claim 27, further comprising a plurality of trace leads located on the base substrate connecting the plurality of bond pads of the first surface of the base substrate and the plurality of bond pads of the second surface of the base substrate.

29. (New) The assembly of claim 22, further comprising:

a base semiconductor die having a plurality of bond pads and disposed on the base substrate first surface; and

a fourth connector connecting the at least one of the plurality of bond pads of the first surface of the base substrate and the at least one bond pad of the base semiconductor die.